Amendments to the Claims

The listing of claims will replace all prior versions, and listings of claims in the application.

1. (Original) A method for supporting serial packet synchronization, comprising the steps of:

in response to receiving a grant, latching a packet sync vector comprised of one or more bits into a serial packet sync transmitter;

loading a preamble comprised of one or more bits into said serial packet sync transmitter, wherein said preamble and said packet sync vector form a serial packet sync datastream;

transmitting said serial packet sync datastream by synchronously shifting each bit of said serial packet sync datastream out of said serial packet sync transmitter;

synchronously receiving each bit of said serial packet sync datastream into a serial packet sync receiver;

latching said packet sync vector into a holding register after comparing each bit of said serial packet sync datastream and determining that said serial packet sync datastream matches said preamble.

2. (Original) The method of claim 1, further comprising the step of generating an interrupt in response to executing said latching step.

3. (Original) The method of claim 1, further comprising the step of transmitting a non-unique bit sequence as said serial packet sync datastream.

4. (Original) The method of claim 1, wherein said transmitting step further comprises the step of synchronizing the transmitting of said serial packet sync datastream to a VoIP clock signal.

5. (Original) The method of claim 1, further comprising the step of preselecting a unique bit sequence as said preamble.

6. (Original) A method for supporting serial packet synchronization, comprising the steps of:

in response to receiving a grant, latching a packet sync vector comprised of one or more bits into a serial packet sync transmitter;

loading a preamble comprised of one or more bits into said serial packet sync transmitter, wherein said preamble and said packet sync vector form a serial packet sync datastream; and

transmitting said serial packet sync datastream by synchronously shifting each bit of said serial packet sync datastream out of said serial packet sync transmitter.

7. (Original) The method of claim 6, further comprising the step of transmitting a non-unique bit sequence as said serial packet sync datastream.

8. (Original) The method of claim 6, wherein said transmitting step further comprises the step of synchronizing the transmitting of said serial packet sync datastream to a VoIP clock signal.

9. (Original) The method of claim 6, further comprising the step of preselecting a unique bit sequence as said preamble.

10. (Original) A method for supporting serial packet synchronization, comprising the steps of:

synchronously receiving each bit of a serial packet sync datastream into a serial packet sync receiver, wherein said serial packet sync datastream is comprised of a packet sync vector and a preamble; and

latching said packet sync vector into a holding register after comparing each bit of said serial packet sync datastream and determining that said serial packet sync datastream matches said preamble.

11. (Original) The method of claim 10, further comprising the step of generating an interrupt in response to said latching step.

12. (Original) A system for supporting serial packet synchronization, comprising:

a media access controller that asserts a packet sync vector in response to receiving a grant;

a serial packet sync encoder that encodes a serial packet sync datastream; and

a serial packet sync receiver that receives said serial packet sync datastream on a single pin.

13. (Original) The system of claim 12, wherein said serial packet sync encoder comprises a serial packet sync transmitter that transmits said serial packet sync datastream on a single pin.

14. (Original) The system of claim 12, wherein said serial packet sync receiver comprises:

a preamble comparator that compares said received serial packet sync datastream to determine if said received serial packet sync datastream matches a preamble; and

a holding register for holding said packet sync vector.

15. (Original) The system of claim 12, wherein said serial packet sync transmitter and said serial packet sync receiver are shift registers.

16. (Original) The system of claim 12, wherein said serial packet sync datastream is comprised of a non-unique bit sequence.

17. (Original) The system of claim 12, wherein after receiving a grant, said serial packet sync datastream is comprised of said packet sync vector and said preamble.

18. (Original) The system of claim 17, wherein said preamble is a preselected unique bit sequence.

19. (Original) A system for transmitting indication of an event, comprising:

a media access controller that asserts a packet sync vector in response to receiving a grant; and

a serial packet sync encoder that encodes a serial packet sync datastream, said serial packet sync datastream comprised of said packet sync vector and a preamble, wherein said serial packet sync encoder comprises a serial packet sync transmitter that transmits said serial packet sync datastream on a single pin as an indication that said grant has arrived.

20. (Original) A system for receiving indication of an event, comprising:

a serial packet sync receiver that receives a serial packet sync datastream on a single pin,

a preamble comparator that compares said received serial packet sync datastream to determine if said received serial packet sync datastream matches a preamble and

a holding register for holding a packet sync vector included in said serial packet sync datastream.